

First CADathlon programming contest held at 2002 ICCAD

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IN THE SPIRIT OF the long-running ACM programming contest, the Special Interest Group on Design Automation (SIGDA) organized an EDA programming contest, the *CADathlon*. SIGDA held the CADathlon on 10 November 2002, at the Double Tree Hotel in San Jose, Calif., as part of the Sunday program for the International Conference on Computer-Aided Design (ICCAD). Students, working in teams of two, competed to solve six problems from different CAD areas. The CADathlon challenged students in their CAD knowledge, and in their problem-solving, programming, and teamworking skills. The contest provided a platform for academia and industry to focus attention on the best and brightest of next-generation CAD professionals. The CADathlon is an innovative initiative that assists in attracting top students to the EDA field.

The students and selection process

The CADathlon competition was open to all graduate students specializing in CAD who were currently enrolled full-time at a PhD-granting institution in any country. Each student team submitted an online appli-

cation. Students provided information about their academic and course backgrounds, and described their three most challenging EDA programming experiences.

Thirty teams applied for the CADathlon, including six non-US teams from Taiwan and Brazil. Organizers ranked students based on their EDA programming experiences, giving preference to more senior students. SIGDA invited 20 teams to participate in the contest, of which 13 received full awards to cover their travel and lodging. Awards went to the most qualified students. Of the 20 teams invited, 15 accepted invitations. SIGDA also gave all participants free ICCAD registration to encourage them to attend the conference and network with the EDA community. Biographies of all participants are available on the CADathlon Web site: <http://www.sigda.org/programs/cadathlon>.

The problems

The CADathlon challenged students in six typical CAD topics. Industrial and academic researchers designed the problems. Table 1 lists these topics.

Organizers imposed a rigorous structure on all problem statements to benefit both the problems' designers and the contestants. Each problem consisted of an introduction, sketching the problem's practical application domain; a problem description, containing all information necessary to understanding and solving the problem; an I/O specification, providing a precise definition of the input and output formats and illustrated with an example; and additional information containing hints and advice on how to tackle the problem or how to use the supplied software. Each problem statement typically amounted to 2 to 4 pages of text, figures, and tables. The "Sample problem: Technology mapping by tree covering" sidebar gives a brief summary of a sample problem.



Participants in the ICCAD 2002 CADathlon.

Sample problem: Technology mapping by tree covering

This problem concerns one of the last steps in logic synthesis: mapping of a gate-level circuit to a library of technology-dependent cells. Several parameters typically characterize the cell library; together, these parameters define the search space for the technology mapper. The mapper's task is to convert the circuit into a functionally equivalent one, solely expressed in library cells, optimizing the design to a certain cost function in the process. A classical paper by Kurt Keutzer accompanied this problem; it set forth the theory involved and a general solution approach. Contestants were to write the code for a technology mapper that would find an area-optimal solution with respect to a prescribed library. As an extra twist, contestants first had to convert the input circuit into a normalized 2-input NAND/INV tree.

Table A shows the given technology-dependent cell library.

Figure A1 shows an example of an input circuit. The actual textual input to the program is

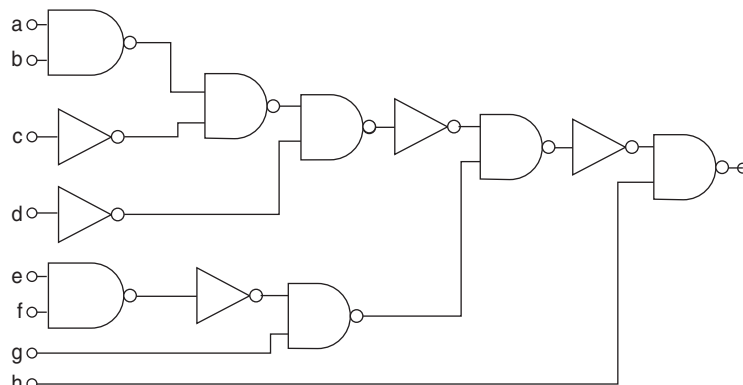
```
! ((! ((a | b) | ! c) | ! d))
| ((! (e | f) | g)) | h
```

where | stands for a 2-input NAND gate and ! represents an inverter.

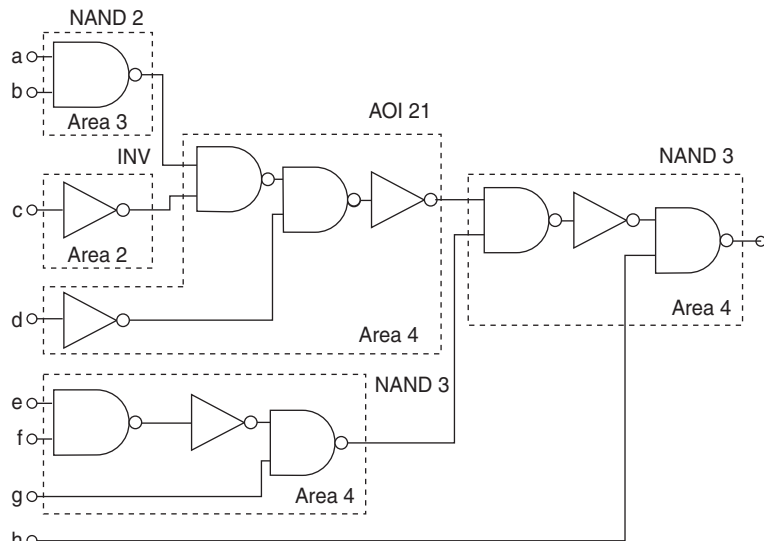
Figure A2 shows a design with a minimum-area result of 17 units. The dashed contours indicate the best-matching library cells.

Table A. Cell library for tree-covering technology mapping.

Cell name	Area (units)	Function	No. of configurations
INV	2	NOT(-)	1
NAND2	3	NAND(-,-)	1
NAND3	4	NAND(-,-,-)	2
NAND4	5	NAND(-,-,-,-)	5
AOI21	4	NOT(OR(-,AND(-,-)))	2
AOI22	5	NOT(OR(AND(-,-),AND(-,-)))	1



(1)



(2)

Figure A. Example input circuit (1) and the same circuit with a minimum-area result of 17 units (2).

Table 1. CADathlon topics.

Topic	Contributor	Affiliation
Analysis and circuit design	Frank Liu	IBM Austin Research Labs
Physical design	Patrick Madden	State University of New York, Binghamton
Logic and high-level synthesis	Geert Janssen	IBM T.J. Watson Research Center
System design and analysis	Sandeep Shukla	Virginia Tech
Functional verification	Geert Janssen	IBM T.J. Watson Research Center
Timing, test, and manufacturing	Soha Hassoun	Tufts University

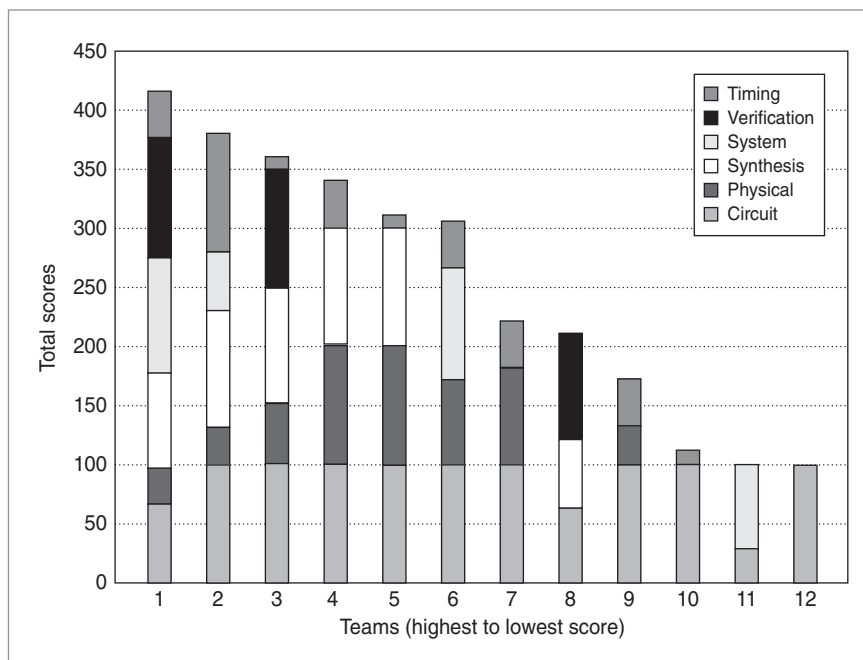


Figure 1. Team results for CADathlon 2002. The total points possible was 600; the maximum possible for each problem was 100.

One week before the contest, the CADathlon Web site posted a research paper related to each of the given problems. Organizers encouraged students to carefully study the papers prior to the contest. Several of the students went so far as to implement the algorithm in the paper to prepare for the contest.

On the day of the contest, SIGDA made the problem statements available both as handouts on paper and in various electronic forms (HTML, Adobe Portable Document Format, and Postscript) on the contestants' computer system. Refer to the CADathlon Web site to view the actual problem statements.

The contest

During the contest, each team worked on a Linux workstation and used three software libraries, includ-

ing GTL, a simple C++ graph template library; the CUDD (Colorado University Decision Diagram) package (in C or C++); and SystemC.

Students had the problem statements and test data samples, but they did not have the judges' full set of test data. Judges evaluated solutions on correctness, and, in the case of the system problem, on efficiency. The team that correctly solved the most problems in the given 10 hours won. Judges did not penalize incorrect solutions.

After the 10-hour programming session, students turned in their electronic solutions. Each problem designer then graded the solutions.

Contest results

Each bar in Figure 1 illustrates the team scores for the six problems. Three of the teams did not complete any problem and thus had a zero score. Almost all

teams solved the problem on analysis and circuit design, the first of the listed problems. Few teams attempted the verification and the system design problems. Only the second-place team correctly solved the timing problem.

SIGDA announced the winners at ICCAD's opening session. In addition to handsome trophies, the first-place team won \$2,000, while the second-place team earned \$1,000.

First-place winners

Matthew R. Guthaus received his BSE in computer engineering and MSE in electrical engineering from the University of Michigan in 1998 and 2000. He is now a PhD candidate in electrical engineering at the University of Michigan, working for Richard Brown. While pursuing his master's degree, Guthaus designed and tested a

mixed-signal, 8-bit microcontroller for sensor and actuator applications. His research interests include standard-cell library optimization, transistor- and gate-level sizing, buffer insertion, and standard-cell placement.

DoRon Motter received his MSE in computer science and engineering from the University of Michigan in May 2002. Motter's graduate research focuses on algorithms for Boolean satisfiability and applications, under Igor Markov. Motter received a BS in computer engineering from the University of Florida (with highest honors) in August 2000; he also has minors in mathematics and physics. In addition, the university named him an Outstanding Four-Year Scholar. Motter's undergraduate thesis was on computationally reversible simulations of quantum particle evolution, work he did with Mike Frank. Currently, Motter is on leave of absence from the University at Microsoft.

Second-place winners

Milos Hrkic received a BS in computer science from the University of Illinois, Chicago. He is pursuing a PhD in computer science at the same university. His research interests include design automation for VLSI, particularly physical design, and timing and combinatorial optimizations. He was also an intern at the IBM Austin Research Laboratory in 2001 and 2002.

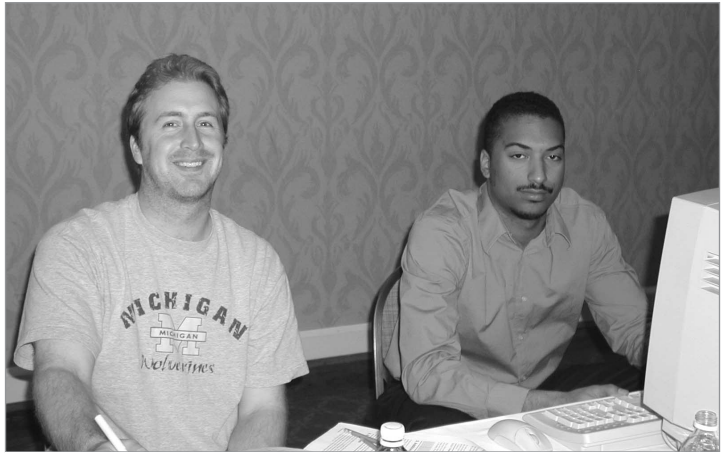
Devangkumar Jariwala received a BE in electrical engineering from the Regional Engineering College, Surat, India. He is now pursuing a PhD in computer science at the University of Illinois, Chicago. His research interests include CAD for VLSI, particularly combinatorial algorithms, and routability analysis and optimizations for placement and floor planning.

The next CADathlon

SIGDA invites students to participate in this year's CADathlon, planned for 9 November 2003; visit <http://www.sigda.org/programs/cadathlon> for details. We invite researchers interested in contributing problems to contact the organizers.

Acknowledgments

The organizers acknowledge the support of many individuals who helped make the CADathlon a success, including Patrick Madden (State University of New York, Binghamton) for many ideas in shaping the CADathlon; Mehmet Yildiz (SUNY, Binghamton) for setting the Linux boxes the day of the context; Andreas Kuehlmann (Cadence Berkeley Labs) for providing earlier input toward making the CADathlon possible;



First-place winners Matthew R. Guthaus (left) and DoRon Motter (right).



Second-place winners Devangkumar Jariwala (left) and Milos Hrkic (right).

the ICCAD executive committee for supporting this effort; and the SIGDA advisory board for its continued support of new outreach programs.

The biography for **Soha Hassoun** appears on page 6 of this issue.



Geert Janssen is a research staff member at IBM's T.J. Watson Research Center. His research interests include hardware verification and logic synthesis. Janssen has an MS in electrical engineering from Eindhoven University, the Netherlands, and a PhD in electrical engineering from the same university. He is a senior member of the IEEE and member of the ACM.